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**★NIDE W01 2000-082166/07 ★JP 11331293-A**

**Phase locked loop circuit for signal estimation device — comprises limitor which suppresses phase shift value of phase difference signal to predetermined fixed value**

NEC CORP 1998.05.11 1998JP-145105

*(1999.11.30) H04L 27/22, H04L 7/00*

NOVELTY - A limiter (107) is provided between phase detector and low pass filter (108), to perform amplitude limitation for the phase difference signal. The phase shift value of phase difference signal is suppressed to a predetermined fixed value. DETAILED DESCRIPTION - The phase of input signal is rotated by a phase rotator (102) and input to a maximum likelihood series estimator (MLSE) (103). A replica signal of input signal is MLSE is generated. The input signal of MLSE is delayed by a delay circuit (104) and it is compared with the replica signal in the phase detector (106) for detecting the phase difference between the two signals. The phase difference signal is filtered and given to the phase rotator through a VCO (109).

**Use:** For signal estimation device.

**Advantage:** PLL operates stably, thus improves estimation capability of MLSE. DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the components of PLL. (102) Phase rotator; (103) MLSE; (104) Delay circuit; (106) Phase detector; (107) Limiter; (108) Low pass filter. (14pp Dwg.No.1/16)

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